

(FILE 'USPAT' ENTERED AT 13:32:05 ON 11 SEP '96)

L1 1019 S TRANSACTION# (3A) (LOAD# OR STORE#)
L2 100196 S BUS##
L3 98 S L1 (P) L2
L4 2 S L3/AB
L5 630195 S BLOCK###
L6 20 S L3 (P) L5
L7 503361 S SPEED
L8 12749 S L2 (P) L7
L9 68 S L3 AND L7
=> d cit l3 1-10

1. 5,555,382, Sep. 10, 1996, Intelligent snoopy bus arbiter; Kurt M. Thaller, et al., 395/293, 280, 299, 458, 473 [IMAGE AVAILABLE]
2. 5,553,266, Sep. 3, 1996, Update vs. invalidate policy for a snoopy bus protocol; Jeffrey A. Metzger, et al., 395/471; 364/228.1, 228.9, 229.2, 243.41, DIG.1; 395/448, 457, 461, 473 [IMAGE AVAILABLE]
3. 5,553,258, Sep. 3, 1996, Method and apparatus for forming an exchange address for a system with different size caches; Nitin D. Godiwala, et al., 395/403; 364/243.44, 254.9, 258.1, DIG.1; 395/421.02, 421.1, 447, 470 [IMAGE AVAILABLE]
4. 5,551,005, Aug. 27, 1996, Apparatus and method of handling race conditions in mesi-based multiprocessor system with private caches; Nitin V. Sarangdhar, et al., 395/472; 364/231.8, 243.44, DIG.1; 395/448, 467, 469, 471, 473 [IMAGE AVAILABLE]
5. 5,548,733, Aug. 20, 1996, Method and apparatus for dynamically controlling the current maximum depth of a pipe lined computer bus system; Nitin Sarangdhar, et al., 395/286; 364/231.8, 240, 240.5, DIG.1; 395/280 [IMAGE AVAILABLE]
6. 5,548,713, Aug. 20, 1996, On-board diagnostic testing; Keith L. Petry, et al., 395/183.01, 183.03, 183.06 [IMAGE AVAILABLE]
7. 5,546,546, Aug. 13, 1996, Method and apparatus for maintaining transaction ordering and arbitrating in a bus bridge; D. Michael Bell, et al., 395/292, 280, 285 [IMAGE AVAILABLE]
8. 5,535,363, Jul. 9, 1996, Method and apparatus for skipping a snoop phase in sequential accesses by a processor in a shared multiprocessor memory system; Paul E. Prince, 395/474, 473, 477 [IMAGE AVAILABLE]
9. 5,533,204, Jul. 2, 1996, Split transaction protocol for the peripheral component interconnect bus; Roger E. Tippley, 395/288, 200.05,